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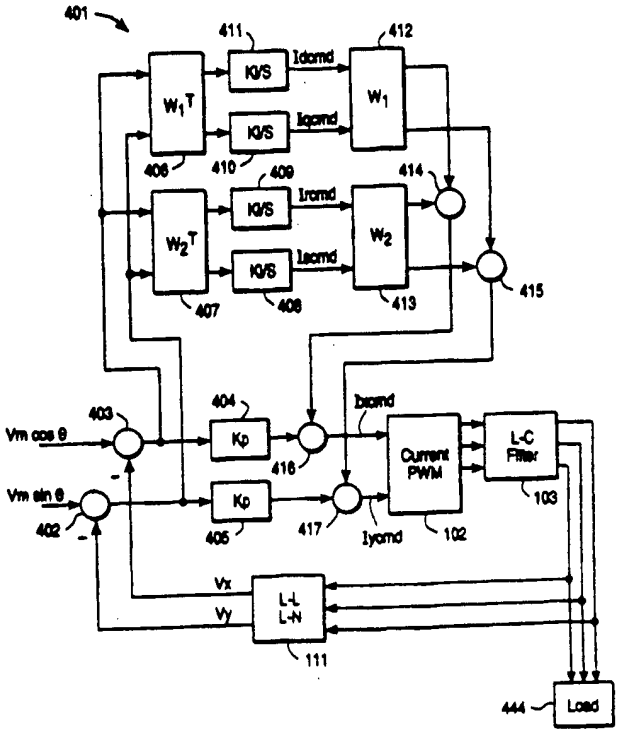
(54) Title: VOLTAGE CONTROLLER FOR SUPPLY OF THREE-PHASE UNBALANCED LOAD FROM STATIC INVERTER

(57) Abstract

A new control scheme for 3-phase inverters that is able to compensate for the effect of load imbalance. In one embodiment, the controller (401) comprises two pairs of PI controllers (404, 405, 408, 409, 410, 411) in two reference frames rotating in opposite directions. These two reference frames extract both positive and negative sequence components of the output voltage. The controller for the negative sequence components effectively compensates for the effect of load imbalance.



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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A 5,329,222 (Gyugyi et al.) 12 July 1994, figs 1a & 1b, col. 5 line 9 - col. 6 line 37	1-16
Y	US, A, 5,187,427 (Erdman), 16 February 1993 col. 4 lines 31- col. 5 line 32.	1-16
A	US, A, 5,001,619 (Nakajima et al.) 19 March 1991	
A	US, A, 5,291,388 (Heinrich) 01 March 1994	
A,P	US, A, 5,436,540 (Kumar) 25 July 1995	

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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VOLTAGE CONTROLLER FOR SUPPLY OF THREE-PHASE UNBALANCED LOAD FROM STATIC INVERTER

FIELD OF THE INVENTION

The present invention relates to the field of control systems for three-phase static power inverters; more particularly, the present invention relates to control schemes that provide a balanced, three-phase voltage source for unbalanced inverter-fed loads.

BACKGROUND OF THE INVENTION

Three-phase inverter-fed loads are very common, particularly in applications such as uninterruptable power supplies (UPS) and remote generation sources (e.g., wind and photovoltaics) above 10 kVA in rating. The six-switch inverter of Figure 1, with its three-wire output, is often the preferred inverter topology due to its low cost. If the loads Za, Zb and Zc, which are delta-connected at the output of the inverter, are balanced, then a variety of control methods exist in the prior art which may be used to regulate the inverter output to a balanced set of line voltages. A commonly used method is the synchronous frame proportional-integral (PI) controller. Such a controller provides good sinusoidal tracking performance without the need for high gain feedback. In a synchronous frame controller, the feedback loop is closed through a rotating reference frame. The rotation frequency of this reference frame is the frequency of the desired output voltage (and current). With respect to this synchronous reference frame, both the feedback variables and the reference variables are direct current

(DC) quantities and, therefore, the integral action of a proportional-integral (PI) controller is able to force the feedback variable to match the reference variable at steady state. However, the integral terms in a typical synchronous frame controller are ineffective for compensating the effect of an unbalanced load.

Figure 2 is a block diagram a typical 3-phase inverter with a synchronous frame voltage controller 101. The objective of controller 101 is to maintain the 3-phase voltage at a certain magnitude and phase relationship regardless of the loading condition. Referring to Figure 2, the output of the controller 101, referred to as Ixcmd 121 and Iycmd 122, are current commands to a pulse-width modulation (PWM) current-regulated voltage source inverter 102. On the feedback path, the line-to-line voltages are converted to their equivalent 2 phase line-to-neutral voltage Vx and Vy using transformation unit 111. The line-to-neutral voltages Vx and Vy are sinusoidal, time varying voltages. These voltages are converted to a synchronous (rotating) frame by frame transformation unit 110 which applies a stationary-to-rotating frame transformation. The resulting voltages output from frame transformation unit 110, Vd and Vq, in ideal circumstances should be constant.

Voltages Vq and Vd are subtracted from 0 and Vm respectively using summing junctions 113 and 114. The values 0 and Vm are reference voltage magnitudes. The outputs of the summing junctions 113 and 114 are tracking errors to control the corrective action of the pair of proportional-integral (PI) controllers.

The tracking error from summing junction 113 is input to integration block 117 of the first PI controller which applies an integral gain constant Ki and an integrator 1/S to the tracking error by multiplying the tracking error by both in order to generate a positive sequence quadrature integral term Vqi. The tracking error from summation junction 113 is also input to the proportional gain block 118 which applies a proportional gain constant (Kp) via multiplication to the tracking error to generate the positive sequence quadrature proportional term Vqp. The positive sequence quadrature integral term Vqi is combined with the positive sequence quadrature proportional term Vqp at summating junction 120, the output of which is sent to frame transformation unit 112.

Similarly, the tracking error output from summing junction 114 is input to integration block 115 and proportional gain block 116 of the second PI controller to generate the positive sequence direct integral term Vdi and the positive sequence direct proportional term Vdp, which are combined at summing junction 119. The result from summing unit 119 is output to frame transformation unit 112. Thus, the outputs from summing junctions 119 and 120 comprise the outputs of the two proportional integral controllers and are the current commands in the synchronous frame. These current commands are transformed back to the stationary frame by frame transformation unit 112 to produce the current commands Ixcmd 121 and Iycmd 122.

For the balanced load case, the current commands Ixcmd 121 and Iycmd 122 are balanced in that they have the same magnitude but are out of

phase with a 90° phase shift with respect to each other. One problem with the synchronous frame controller in Figure 2 is that, with zero tracking error, it is only capable of providing balanced current commands. That is, current commands Ixcmd 121 and Iycmd 122 can only be balanced currents.

The current commands 121 and 122 are input to PWM current-regulated voltage source inverter 102 which generates outputs which are input to L-C filter 103. L-C filter 103 eliminates line current harmonics and may be used to increase power factor. The outputs of L-C filter 103 are supplied to load 104.

Figure 3 shows a delta-connected load. In the case of a balanced load (i.e., Za=Zb=Zc), the 2-phase current vector and voltage vector are related by equation (1) below. In this case, to produce a balanced voltage, Ix and Iy must have the same magnitude and must be 90^{O} apart.

$$\begin{pmatrix} Ix \\ Iy \end{pmatrix} = \begin{pmatrix} 3/Z & 0 \\ 0 & 3/Z \end{pmatrix} \cdot \begin{pmatrix} Vx \\ Vy \end{pmatrix} \qquad (1)$$

Equation (2) below shows the relationship between the current and the voltage vector in the unbalanced case.

$$\begin{pmatrix} Ix \\ Iy \end{pmatrix} := \begin{bmatrix} \frac{3}{2} \cdot \frac{(Zc + Za))}{ZaZc} & \frac{1}{2} \cdot \sqrt{3} \cdot \frac{(-Zc + Za)}{ZaZc} \\ \frac{1}{2} \cdot \sqrt{3} \frac{(-Zc + Za)}{ZaZc} & \frac{1}{2} \cdot \frac{((ZcZb + ZbZa + 4ZaZc)}{ZaZcZb} \end{bmatrix} \begin{pmatrix} Vx \\ Vy \end{pmatrix} \qquad (2)$$

Since the impedance matrix is no longer diagonal, to produce a balanced voltage, the magnitude and relative phase of Ix and Iy must be adjusted according to the load. This situation is depicted in Figure 4.

Figure 4 shows the phase relation between Iy and Ix under various loading conditions for a given balanced voltage. Trace 1 (circular trajectory) is the balanced case (i.e., Za=Zb=Zc as in Figure 3). The per-phase impedance is a 300uF capacitor (for filtering) in parallel with a 2Ω resistor at 60Hz. Traces 2 is the case where the resistors in Za remains to be 2Ω but the resistors in Zb and Zc are changed to 200Ω. The loading conditions that generate trace 3 and 4 are similar to the load that generates trace 2 except that a 2Ω resistor is connected in Zb (for trace 3) and Zc (for trace 4) and 200Ω on the other two legs.

Note that the circular trajectory 1 in Figure 3 can be produced by a constant 2 dimensional vector in the synchronous frame. This two-dimensional (2D) vector is precisely the value to which the integral terms (i.e., [Vdi, Vqi] in Figure 2) will converge. For a heavier load, the magnitude of the vector [Vdi, Vqi] converges to a higher value. For a reactive load, the angle of the vector [Vdi, Vqi] converges to the phase angle of the load. This vector allows a two degree-of-freedom adjustment of the current commands Ixcmd and Iycmd, i.e., (a) the magnitude of both Ixcmd and Iycmd and (b) their phase angle with respect to the voltage angle (θ). The magnitude of the current commands Ixcmd and Iycmd cannot be adjusted individually and the relative angle between Ixcmd and Iycmd is

fixed at 90^{o} regardless of the value of Vdi and Vqi as shown in the frame transformation equation (3) below.

$$\begin{pmatrix} Ixcmd \\ Iycmd \end{pmatrix} = \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix} \cdot \begin{pmatrix} Vdi \\ Vqi \end{pmatrix} \qquad (3)$$

From Figure 2, it is clear that this adjustment is provided by the proportional terms (Vdp and Vqp), which are derived from the instantaneous voltage error. In this case, the proportional gain constant (Kp) must be sufficiently high in order to keep the voltage error below a certain level. In practical systems, the proportional gain is often limited by the stability margin and, therefore, unable to adequately compensate for the effect of load imbalance.

An alternate approach for compensating for load imbalance is shown in Figure 5. Referring to Figure 5, three single phase inverters are delta-connected, and each inverter is independently controlled via a very simple voltage regulator such as that shown in Figure 6. The advantage of this approach over the three-phase, six-switch inverter of Figure 1 controlled by the synchronous frame PI controller of Figure 2 is that the system of single phase inverters can support any amount of load imbalance while maintaining balanced three-phase voltages. Further, a wye connection allows for a neutral conductor to be extended to the load, providing four-wire service for single-phase, line-to-neutral connected loads, as shown in Figure 7. The obvious disadvantage is higher cost, with twice the number of power semiconductors and three single-phase transformer required, rather than the single three-phase transformer required in Figure 2.

Recent research works related to this subject include Dixon, Garcia, and Moran, "Control System for Three-Phase Active Power Filter Which Simultaneously Compensates Power Factor and Unbalanced Loads", *IEEE Trans. on Industrial Electronics*, Vol. 42, No. 6, Dec. 1995, pp. 630-636 and Verdelho and Marques, "An Active Power Filter and Unbalanced Current Compensator", *IEEE Trans. on Industrial Electronics*, Vol. 44, No. 3, June 1997, pp. 308-321. For an explanation of the application of symmetrical components to the analysis of unbalanced three-phase power systems, see W. D. Stevenson, *Elements of Power System Analysis, 4th Edition*, chap. 11, McGraw-Hill, New York, 1982.

SUMMARY OF THE INVENTION

A control scheme is described. The control scheme may be used to provide a balanced, three-phase set of voltages to an unbalanced load, which may be in either a three-wire or a four-wire configuration. In one embodiment, the control scheme is a 3-phase synchronous control scheme for an unbalanced load. Such a load may be supplied by a static power inverter. The control scheme uses two pairs of PI controllers situated in reference frames rotating in opposite directions. One of the pairs of PI controllers regulates positive sequence components and the other pair of PI controllers regulates negative sequence components.

In one embodiment, one of the pairs of PI controllers regulates positive sequence load currents to produce a desired positive sequence

voltage, while the other pair of PI controllers regulates negative sequence load currents to compensate for the effect of an unbalanced load.

In another embodiment, the control scheme uses a single pair of proportional controllers situated in a single stationary reference frame, with high proportional gains selected to reduce voltage tracking errors to acceptable levels. In this embodiment, lead-lag compensators are utilized at the outputs of the proportional controllers to counteract the destabilizing effect of the high proportional gain.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

Figure 1 is a block diagram of a 3-phase, 3-wire balanced load being fed by a three-phase inverter.

Figure 2 is a block diagram of a typical 3-phase inverter with a synchronous frame voltage controller.

Figure 3 illustrates a delta-connected load.

Figure 4 illustrates the phase relation between Iy and Ix under various loading conditions for a given balanced voltage.

Figure 5 is a block diagram illustrating a 3-phase, 3-wire unbalanced load being fed by three single-phase inverters.

Figure 6 is a block diagram illustrating a voltage controller for a single-phase inverter that may be used to control a single-phase inverter shown in **Figures 5 and 7**.

Figure 7 is a block diagram illustrating a 3-phase, 4-wire unbalanced load being fed by three single-phase inverters.

Figure 8 is a block diagram of one embodiment of a synchronous frame controller for unbalanced loads.

Figure 9 is a block diagram of a control structure with the proportional terms in the synchronous frame.

Figure 10 is a block diagram of a 3-phase, 3-wire unbalanced load being fed by three-phase inverter controlled by a synchronous frame controller.

Figure 11 is a block diagram of a 3-phase, 4-wire unbalanced load being fed by three-phase inverter controlled by a synchronous frame controller.

Figure 12 is a block diagram of a stationary frame proportional voltage controller.

Figure 13 is a block diagram of a stationary frame proportional voltage controller with lead-lag compensation.

DETAILED DESCRIPTION

A control scheme is described. In the following description, numerous details are set forth such as, for example, specific frequencies, specific proportional gain values, specific integral values etc. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

Some portions of the detailed descriptions which follow are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to

be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

The present invention also relates to apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the

computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, and magneto-optical disks, read-only memories (ROMs), random access memories (RAMs), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, and each coupled to a computer system bus. The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose machines may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these machines will appear from the description below. In addition, the present invention is not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of the invention as described herein.

All or a portion of the operations described herein may be performed by analog or digital circuitry and/or logic.

Overview

A controller compensates for the effect of load imbalance. In one embodiment, the controller has two pairs of PI controllers in two reference frames rotating in the opposite directions. These two reference frames extract both positive and negative sequence components of the output

voltage. The pair of PI controllers in the reference frame that rotates in the same direction as the desired output voltage vector regulates the positive sequence components of the output voltage. In one embodiment, this pair of PI controllers regulates the positive sequence load currents to produce the desired positive sequence voltage. The other pair of PI controllers regulates the negative sequence components. In one embodiment, this pair of PI controllers regulates the negative sequence load currents. The controller for the negative sequence components compensates for the effect of load imbalance. The controller may be a synchronous frame controller using two PI compensators in separate reference frames with opposite rotation.

In another embodiment, the control scheme uses a single pair of proportional controllers situated in a single stationary reference frame, with high proportional gains selected to reduce voltage tracking errors to acceptable levels. In one embodiment, lead-lag compensators are utilized at the outputs of the proportional controllers to counteract the destabilizing effect of the high proportional gain. The controller may be a synchronous frame controller in a single rotating reference frame using lead-lag compensation.

Table 1 sets for the meanings to variable names that are used herein.

Table 1 Variable names and their definitions.

Variable Names	Meaning
Kp	Proportional gain constant
Ki	Integral gain constant
1/S	Integrator

θ	$= 2\pi ft$
f	Line frequency (e.g., 60 Hz)
Vab, Vbc, Vac	3-ϕ line-to-line voltage
Vx, Vy	x and y component of 2-ϕ voltage
V m	reference voltage magnitude
Vd, Vq	Direct and quadrature axis voltage components (positive seq. components)
Vr, Vs	Direct and quadrature axis voltage components (negative seq. components)
Vxerr, Vyerr	x, y components of the voltage error in the stationary frame
Vderr, Vqerr	Positive sequence voltage error
Vrerr, Vserr	Negative sequence voltage error
Vdi, Vqi	Positive sequence integral terms
Vri, Vsi	Negative sequence integral terms
Vdp, Vqp	Direct and quadrature proportional terms
Ixcmd, Iycmd	stationary frame current command
Ix, Iy	stationary frame 2-ϕ current
Ia, Ib, Ic	stationary frame 3-ϕ current
$W_1(\theta)$	Positive sequence component transformation matrix
$W_2(\theta)$	Negative sequence component transformation matrix

As shown in Figure 4, in the case of load imbalance, the relative magnitude and angle of Ixcmd and Iycmd must be adjusted in order to keep the 3-phase voltage balanced. To generate an ellipse of arbitrary magnitude and phase angle (as traces 2-4 in Figure 4), a four degree-of-freedom adjustment may be employed as described in the following section. Figure 8 is a block diagram of one embodiment of such a controller.

Referring to Figure 8, the line-to-line voltage is converted to its equivalent 2-ϕ line-to-neutral voltages Vx and Vy. The y component of the 2-ϕ voltage is subtracted from the reference voltage $Vm\sin(\theta)$ at summing

junction 402 to create a first tracking error. The first tracking error is sent to proportional gain block 405 and one input of $W_1^T(\theta)$ block 406 and one input of $W_2^T(\theta)$ block 407. Similarly, the x component of the 2-ϕ voltage is subtracted from the reference voltage $Vm\cos(\theta)$ at summing junction 403. The output of summing junction 403 is a second tracking error that is forwarded to proportional gain block 404 and the other input of blocks 406 and 407. The first and second tracking errors are in the stationary frame.

Proportional gain blocks 404 and 405 multiply the tracking errors output from summing junctions 403 and 402, respectively, by a proportional gain constant Kp so as to magnify the tracking error proportionally with a constant. The proportional gain constant Kp is highly application dependent and varies based on inverter rating and desired dynamic response, among other considerations. The result of the multiplications performed by proportional gain blocks 404 and 405 are output to summing junctions 416 and 417, respectively, for combining with the outputs of summing junctions 414 and 415, respectively.

$W_1^T(\theta)$ block 406 applies the transpose of the transformation matrix $W_1(\theta)$ to the tracking errors output from summing junctions 403 and 402. The result of applying the transpose of the transformation matrix $W_1(\theta)$ is a first voltage error vector in the synchronous frame. The first voltage error vector is sent to a pair of integration blocks, 411 and 410, of a pair of PI controllers. Integration blocks 411 and 410 apply an integral gain constant Ki and an integrator 1/S to different individual values of the first voltage

error vector. The integral gain constant Ki is application dependent. Each integration block multiplies the integral gain constant Ki and the integrator 1/S to the value of the first voltage error vector. The outputs of integration blocks 410 and 411 comprise integral terms in the synchronous frame and are input to $W_1(\theta)$ block 412. $W_1(\theta)$ block 412 applies the transformation matrix $W_1(\theta)$ to its inputs to convert the integral terms to the stationary frame. The integral terms in the stationary frame are input to summing junctions 414 and 415.

$W_2^T(\theta)$ block 407 applies the transpose of the transformation matrix $W_2(\theta)$ to the tracking errors output from summing junctions 403 and 402. The result of applying the transpose of the transformation matrix $W_2(\theta)$ is a second voltage error vector in the synchronous frame. The second voltage error vector is sent to a pair of integration blocks 409 and 408 of a pair of PI controllers. Integration blocks, 409 and 408, apply an integral gain constant Ki and an integrator 1/S to different individual values of the second voltage error vector. Each of integration blocks 408 and 409 multiplies the integral gain constant Ki and the integrator 1/S to the value of the second voltage error vector. The outputs of integration blocks 409 and 408 comprise integral terms in the synchronous frame and are input of $W_2(\theta)$ block 413. $W_2(\theta)$ block 413 applies the transformation matrix $W_2(\theta)$ to its inputs to convert the integral terms to the stationary frame, which are coupled to inputs of summing junctions 414 and 415.

The value of Kp and Ki may vary over a wide range. They may depend mainly on the power and voltage rating of the system. They may also depend on the characteristics of the hardware on which this control scheme is implemented. In a 200~300kw system, a typical Kp value is 1 and for Ki is about 10. These are conservative values. It is possible to have these values increased 5 times with some tuning. Note that in one embodiment, the gains in both reference frames are the same; however, the gains may be different. In one embodiment, the integrator 1/S functions as an accumulator.

Summing junction 414 sums one output of $W_1(\theta)$ block 412 to one output of $W_2(\theta)$ block 413 to produce a result that is input to one input of summing junction 416. Summing junction 415 sums the other output of $W_1(\theta)$ block 412 to the other output of $W_2(\theta)$ block 413 to produce a result which is input to summing junction 417.

Summing junction 416 generates a sum corresponding to the x component of the stationary frame current command, i.e., the Ixcmd current command. Summing junction 417 generates the y component of the stationary frame current command i.e., the Iycmd current command. The stationary frame current commands Ixcmd and Iycmd are input to the PWM current-regulated voltage source inverter 102 which generates outputs which are input to L-C filter 103. In one embodiment, Ixcmd and Iycmd are two current commands, with 90 degree phase displacement, that

are summed to form a single current command. The outputs of L-C filter 103 are supplied to load 444.

Integration blocks 408-411 and proportional gain blocks 404-405 form the two pairs of PI controllers. The proportional terms applied by proportional gain blocks 404 and 405 are in the stationary frame. Also, the four integral terms produced by integration blocks 408-411 allow independent adjustment of the magnitude and phase of both the x and y components of the stationary frame current command.

Each summing junction may comprise hardware, such as an adder, a subtractor, a comparator, dedicated hardware unit, or a general purpose arithmetic unit, or may comprise software for execution on a dedicated or general purpose machine, or a combination of both.

In the synchronous controller shown in Figure 8, the current commands are calculated according to equation (4) given below. Definitions of the variables used in equation (4) are given in Table 1 and equations (5) - (11).

$$\begin{pmatrix} Ixcmd \\ Iycmd \end{pmatrix} = Kp\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix} + KiW_1(\theta)\begin{pmatrix} Vdi \\ Vqi \end{pmatrix} + KiW_2(\theta)\begin{pmatrix} Vri \\ Vsi \end{pmatrix} \quad (4)$$

$$Vxerr = Vm\cos(\theta) - Vx \quad (5)$$

$$Vyerr = Vm\sin(\theta) - Vy \quad (6)$$

$$W_1(\theta) := \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix} \quad (7)$$

$$W_2(\theta) := \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ -\sin(\theta) & -\cos(\theta) \end{pmatrix} \quad (8)$$

$$Vdi = \int Vderrdt \quad Vri := \int Vrerrdt$$
$$Vqi = \int Vqerrdt \quad Vsi := \int Vserrdt \quad (9)$$

$$\begin{pmatrix} Vderr \\ Vqerr \end{pmatrix} = W_1(\theta)^T\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix} \quad (10)$$

$$\begin{pmatrix} Vrerr \\ Vserr \end{pmatrix} = W_2(\theta)^T\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix} \quad (11)$$

The transformation matrix $W_1(\theta)$ corresponds to a rotating frame that is in sync with the desired output voltage and hence the variables Vderr and Vqerr are the direct and quadrature components of the positive sequence voltage error. The transformation matrix $W_2(\theta)$ corresponds to a rotating frame that is also in sync with the desired output voltage but the rotation is in the opposite direction and, therefore, Vrerr and Vserr are the direct and quadrature components of the negative sequence voltage error. The meaning of the negative sequence integral terms Vri and Vsi can

be seen from equation (12). In equation (12), x and y components of the voltage error in the stationary frame, referred to as Vxerr and Vyerr, are represented by two sinusoidal functions with arbitrary magnitude (vxerr and vyerr) and phase (ϕx and ϕy). Since the integral action is slow, the integral terms can be thought of as an averaged value of the input. From the averaged value (12) of the transformed Vxerr and Vyerr, it is clear that, if vxerr=vyerr and ϕx=ϕy (i.e., balanced load condition), Vri and Vsi will not contribute to Ixcmd and Iycmd.

$$\begin{aligned}\begin{bmatrix} Vri \\ Vsi \end{bmatrix} &= \frac{Ki}{2\pi}\int_0^{2\pi}\begin{bmatrix} \cos\theta & -\sin\theta \\ -\sin\theta & -\cos\theta \end{bmatrix}\begin{bmatrix} vxerr\cdot\cos(\theta+\phi x) \\ vyerr\cdot\sin(\theta+\phi y) \end{bmatrix}dt \\ &= \frac{1}{2}\begin{bmatrix} vxerr\cdot\cos(\phi x) - vyerr\cdot\cos\phi y \\ vxerr\cdot\sin(\phi x) - vyerr\cdot\sin\phi y \end{bmatrix} \\ &= \begin{bmatrix} 0 \\ 0 \end{bmatrix}\end{aligned} \qquad (12)$$

Note that, unlike in the controller shown in Figure 2, in the controller in Figure 8, the proportional terms are placed in the stationary frame. These proportional terms can also be placed in the synchronous frame as shown in Figure 9.

Referring to Figure 9, the line-to-line voltage is converted to its equivalent 2-ϕ phase line-to-neutral voltages Vx and Vy. The x and y components of the 2-ϕ voltage are both inputs to $W_1^T(\theta)$ block 406 and $W_2^T(\theta)$ block 407 which apply the transpose of the transformation matrices

$W_1(\theta)$ and $W_2(\theta)$, respectively, to these inputs. Thus, the x and y components of the 2-ϕ voltage are transformed into the synchronous frame.

The outputs of $W_1^T(\theta)$ block 406 are subtracted from the reference voltage magnitudes Vm and 0 using summing junctions 501 and 502, respectively. The results of the subtractions are tracking errors in the positive sequence synchronous frame and are output from summing junctions 501 and 502 to PI controllers 505 and 506, respectively.

PI controllers 505 and 506 regulate the positive sequence components. PI controller 505 applies a proportional gain constant Kp to the first tracking error. In one embodiment, PI controller 505 multiplies the proportional gain constant Kp to the tracking error. PI controller 505 adds the result of the multiplication to the result of applying an integral gain constant Ki, multiplied by an integrator 1/S, to the first tracking error. The result of the addition is an integral term in the synchronous frame and is input to $W_1(\theta)$ block 412.

Similarly, PI controller 506 applies a proportional gain constant Kp to the second tracking error by multiplying the proportional gain constant Kp to the tracking error. PI controller 506 adds the result of the multiplication to the result of applying the integral gain constant Ki, multiplied by the integrator 1/S, to the second tracking error. The results of the addition is an integral term in the synchronous frame and is input to $W_1(\theta)$ block 412. $W_1(\theta)$ block 412 applies the transformation matrix $W_1(\theta)$ to the outputs of PI controllers 505 and 506 to generate integral terms in the stationary frame.

These integral terms in the stationary frame are sent to summing junctions 509 and 510.

The outputs of $W_2^T(\theta)$ block 407 are subtracted from the reference voltage magnitudes Vmcos(2θ) and -Vmsin(2θ) using summing junctions 503 and 504, respectively. The results of the subtractions are tracking errors in the negative sequence synchronous frame and are output from the summing junctions 503 and 504 to PI controllers 507 and 508, respectively.

PI controllers 507 and 508 regulate the negative sequence components. PI controller 507 applies a proportional gain constant Kp to the third tracking error. In one embodiment, PI controller 507 multiplies the third tracking error by the proportional gain constant Kp. PI controller 507 adds the result of the multiplication to the result of applying an integral gain constant Ki, multiplied by an integrator 1/S, to the third tracking error. The result of the addition is an integral term in the synchronous frame and is input to $W_2(\theta)$ block 413.

Similarly, PI controller 508 applies the proportional gain constant Kp to the fourth tracking error by multiplying the fourth tracking error by the proportional gain constant Kp. PI controller 508 adds the result of the multiplication to the result of applying the integral gain constant Ki, multiplied by the integrator 1/S, to the fourth tracking error. The results of the addition is an integral term in the synchronous frame and is input to $W_2(\theta)$ block 413. $W_2(\theta)$ block 413 applies the transformation matrix $W_2(\theta)$ to the outputs of PI controllers 507 and 508 to generate integral terms in the

stationary frame. The integral terms in the stationary frame are sent to summing junctions 509 and 510.

Summing junctions 509 and 510 combine integral terms in the stationary frame to generate the current commands Iycmd and Ixcmd. These commands are forwarded onto a PWM current-regulated voltage source inverter coupled to an L-C filter, shown as block 520, the outputs of which are supplied to load 444.

As shown in Figures 9 and 2, the d and q component of the reference voltage should be Vm and 0. The voltage reference for the r and s axis can be derived from transforming the sinusoidal reference to the negative sequence reference frame as shown in equation (13) below.

$$\begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ -\sin(\theta) & -\cos(\theta) \end{pmatrix}^{T} \cdot \begin{pmatrix} Vm \cdot \cos(\theta) \\ Vm \cdot \sin(\theta) \end{pmatrix} = \begin{pmatrix} Vm \cdot \cos(2 \cdot \theta) \\ -Vm \cdot \sin(2 \cdot \theta) \end{pmatrix} \qquad (13)$$

Since $W_1(\theta)$ and $W_2(\theta)$ are inverses of $W_1^T(\theta)$ and $W_2^T(\theta)$, the controllers shown in Figure 8 and Figure 9 are, in fact, functionally equivalent.

Embodiments of controllers described herein may be used in the systems shown in Figure 10 and 11. Figure 10 is a block diagram of a 3-phase, 3-wire unbalanced load being fed by three-phase inverter controlled by a synchronous frame controller. Figure 11 differs from Figure 10 in that it includes a 4-wire load instead of a 3-wire load. Figure 11 will only be described to the extent the system depicted therein differs from Figure 10. It is important to note that in Figure 11 the transformer is delta-wye

connected, which allows the three-wire inverter output to serve a four-wire load.

Referring to Figure 10, an inverter 1052 comprising active switching devices 1056 coupled to gate drivers 1053 is shown. In one embodiment, the inverter 1052 includes three pairs of active switching devices 1056 arranged in a bridge circuit. The intermediate points of the pairs of active switching devices 1056 form three output taps from which three phase electricity flows through the filters 1051 and transformer 1050 to load 1055 (e.g., the utility grid). Commutation signals for the active switching devices 1056 originate in inverter controller 1054, which supplies the signals to the switching devices through gate driver 1053. In one embodiment, inverter controller and gate driver 1053 are isolated from inverter 1052 by optical isolators. The commutation signals are complementary for each pair of switching devices, causing one switching device of each pair to switch on and the other switching devices of the pair to switch off at any given time. In one embodiment, switching devices 1056 of inverter 1052 comprises six IGBT's arranged in parallel pairs.

Switching devices 1056 can be any of a number of differently types of active switches, including insulated gate bipolar transistors (IGBT), bipolar junction transistors, field effect transistors, darlington transistors, gate turn-off thyristors, or silicon controlled rectifiers.

In one embodiment, inverter controller 1054 comprises a PWM current-regulated inverter and generates pulse width modulated commutation signals and supplies them to inverter switches 1056 through

the drive circuit 1053. This PWM current-regulated inverter may generate these signals in response to a synchronous frame controller described herein.

Figure 12 is a block diagram of an embodiment of a stationary frame proportional voltage controller that does not adequately compensate for load imbalance. Referring to Figure 12, the measured output voltage is first converted to its 2-phase equivalent (Vx and Vy) by transformation unit 111. The voltages Vx and Vy are compared against two reference signals (Vxref and Vyref) using summing junctions 1004 and 1005 respectively. In one embodiment, these reference signals are 60Hz sinusoidal functions and are 90° apart. The differences between the measured voltage (Vx and Vy) and the reference signal (Vxref and Vyref) are the tracking errors Vex and Vey and are output of summing junctions 1004 and 1005 respectively. The control output is derived from multiplying the tracking errors by a proportional gain (Kp) using proportional gain blocks 1002 and 1003. With this feedback loop, the controller is able to force the output voltage to follow the reference sinusoidal signals under various loading conditions. In general, the higher the proportional gain Kp, the closer tracking can be achieved. In the case of a severe load imbalance condition, a high value of Kp is necessary to keep the output voltage from deviating too far from the nominal value.

The output of proportional gain blocks 1002 and 1003 are the current commands in the synchronous frame. These current commands are transformed back to the stationery frame by frame transformation unit 1001.

The current commands are input to PWM current-regulated voltage source inverter 102 which generates outputs which are input to L-C filter 103. The outputs of L-C filter 103 are supplied to load 444.

In a practical system, Kp must be kept below a maximum value in order to preserve the control loop's stability. It is often the case that this maximum value is lower than the value of Kp that is necessary to compensate for load imbalance. The maximum value Kp for stability depends on the loop frequency response. Figure 13 illustrates a synchronous frame controller in a single rotating reference frame using lead-lag compensation. In Figure 13, two lead-lag compensators 1010 and 1011 are applied to the output of the proportional gain blocks. The purpose of compensators 1010 and 1011 is to shape the frequency response so that the maximum value of Kp can be extended to a higher value. The lead-lag compensators shape the frequency response by introducing poles and zeroes which increase the phase margin of the closed loop response of the system.

In one embodiment, the gains in both reference frames are the same; however, the gains may be different.

Note that this control scheme may also be used as part of the inverter controllers in Figures 10 and 11.

It should be noted that embodiments described herein may be implemented, fully or in part, using analog and/or digital circuits, or may be implemented with a digital signal processor or other processing device, general or dedicated, executing code or other executable instructions. Some or all of the functionality of the controller may be implemented in software

that executes on one or more general purpose or dedicated processing devices (e.g., processor, controller, etc.).

Thus, various control scheme embodiments have been described. The control scheme embodiments may provide control for inverter applications that require a regulated, balanced set of three-phase output voltages in the presence of unbalanced loads. These would include, but are not limited to, back-up power and power quality applications, such as, for example, uninterruptable power supplies (UPS), which are powered by batteries, flywheels, supercapacitors or superconducting magnets, and distributed, stand-alone power systems with generation sources such as, for example, solar photovoltaics, wind turbines or fuel cells.

In one embodiment, operations described herein are carried out in a computer system in response to its central processing unit (CPU) executing sequences of instructions contained in a memory, which may be random access memory (RAM). That is, execution of the sequences of instructions contained in memory causes the CPU to perform the operations, which will be described below. The instructions may be loaded into memory from a persistent store, such as a mass storage device or any one of the memories described above.

In alternative embodiments, hardwired circuitry may be used in place of, or in combination with, software instructions to implement the operations. Thus, the present invention is not limited to any specific combination of hardware circuitry and software.

Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as essential to the invention.

Thus, a control scheme has been described.

CLAIMS

We claim:

1. A synchronous frame controller comprising two pairs of PI controllers situated in two reference frames rotating in opposite directions, wherein one of the two pairs of PI controllers regulates positive sequence components and the other of the two pairs of PI controllers regulates negative sequence components.

2. The controller defined in Claim 1 wherein the one of the two pairs of PI controllers is in the reference frame that rotates in the same direction as a desired output voltage vector.

3. The controller defined in Claim 1 wherein the two reference frames extract both positive and negative components of an output voltage.

4. The controller defined in Claim 1 wherein the other of the two pairs of PI controllers controls the negative sequence components to compensate for effects of load imbalance.

5. The controller defined in Claim 1 wherein the two pairs of PI controllers generate unbalanced currents.

6. The controller defined in Claim 1 wherein the proportional terms are in the synchronous frame.

7. The controller defined in Claim 1 wherein the proportional terms are in the stationary frame.

8. The controller defined in Claim 1 wherein four integral terms of the two pairs of PI controllers allow independent adjustment of magnitude and phase of commanded unbalanced currents.

9. A synchronous frame controller comprising two pairs of PI controllers, one of the two pairs of PI controllers regulating positive sequence load currents to produce the desired positive sequence voltage and the other of the two pairs of PI controllers regulates negative sequence load currents to compensate for an effect of an unbalanced load.

10. The controller defined in Claim 9 wherein the proportional terms are in the synchronous frame.

11. The controller defined in Claim 9 wherein the proportional terms are in the stationary frame.

12. The controller defined in Claim 9 wherein four integral terms of the two pairs of PI controllers allow independent adjustment of magnitude and phase of commanded unbalanced currents.

13. A system comprising:

a load;

a filter coupled to the load;

a current-regulated voltage source inverter coupled to the filter;

a controller coupled to the load and the current-regulated voltage source inverter, the controller comprising two pairs of PI controllers, one of the two pairs of PI controllers regulating positive sequence load currents to produce the desired positive sequence voltage and the other of the two pairs of PI controllers regulates negative sequence load currents to compensate for an effect of an unbalanced load.

14. The system defined in Claim 13 wherein the load comprises a 3-wire load.

15. The system defined in Claim 13 wherein the load comprises a 4-wire load.

16. The system defined in Claim 13 wherein the filter comprises an L-C filter.

17. The system defined in Claim 13 wherein the current amplifier comprises a PWM current amplifier.

18. The system defined in Claim 13 wherein the one of the two pairs of PI controllers is in the reference frame that rotates in the same direction as a desired output voltage vector.

19. The system defined in Claim 13 wherein the two reference frames extract both positive and negative components of an output voltage.

20. The system defined in Claim 13 wherein the other of the two pairs of PI controllers controls the negative sequence components to compensate for effects of load imbalance.

21. The system defined in Claim 13 wherein the proportional terms are in the synchronous frame.

22. The system defined in Claim 13 wherein the proportional terms are in the stationary frames.

23. The system defined in Claim 13 wherein four integral terms of the two pairs of PI controllers allow independent adjustment of magnitude and phase of commanded unbalanced currents.

24. The system defined in Claim 13 wherein the controller produces an output comprising current commands.

25. The system defined in Claim 13 wherein the controller calculates current commands Ixcmd and Iycmd according to the following:

$$\begin{pmatrix} Ixcmd \\ Iycmd \end{pmatrix} = Kp\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix} + KiW1(\theta)\begin{pmatrix} Vdi \\ Vqi \end{pmatrix} + KiW2(\theta)\begin{pmatrix} Vri \\ Vsi \end{pmatrix}$$

$$Vxerr = Vm\cos(\theta) - Vx$$

$$Vyerr = Vm\sin(\theta) - Vy$$

$$W1(\theta) := \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix}$$

$$W2(\theta) := \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ -\sin(\theta) & -\cos(\theta) \end{pmatrix}$$

$$Vdi = \int Vderrdt \quad Vri := \int Vrerrdt$$

$$Vqi = \int Vqerrdt \quad Vsi := \int Vserrdt$$

$$\begin{pmatrix} Vderr \\ Vqerr \end{pmatrix} = W1(\theta)^T\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix}$$

$$\begin{pmatrix} Vrerr \\ Vserr \end{pmatrix} = W2(\theta)^T\begin{pmatrix} Vxerr \\ Vyerr \end{pmatrix}$$

26. A controller comprising:

a pair of proportional controllers, situated in the synchronous frame, to apply a proportional gain constant to a pair of tracking errors to generate a pair of commands;

a pair of compensators to generate compensated versions of the pair of commands in response thereto;

a frame transformation unit to convert the compensated versions of the pair of commands to the stationary frame, the frame transformation unit output the converted compensated versions of the pair of commands for control.

27. The controller defined in Claim 26 wherein each of the pair of compensators comprises a lead-lag compensator.

28. The controller defined in Claim 26 wherein the pair of compensators counteract a destabilizing effect of proportional gains associated with the pair of proportional controllers.

29. The controller defined in Claim 26 wherein the proportional gains reduce voltage tracking errors to a predetermined level.

30. A system comprising:

a pair of proportional controllers, situated in the synchronous frame, to apply a proportional gain constant to a pair of tracking errors to generate a pair of commands;

a pair of compensators to generate compensated versions of the pair of commands in response thereto;

a frame transformation unit to convert the compensated versions of the pair of commands to the stationary frame;

a current-regulated voltage source inverter responsive to the converted compensated versions of the pair of commands to for supplying output electricity; and

a load coupled to the inverter.

31. The system defined in Claim 30 wherein the load comprises a 3-wire load.

32. The system defined in Claim 30 wherein the load comprises a 4-wire load.

33. The system defined in Claim 30 wherein the inverter comprises a PWM current-regulated voltage source inverter.

34. The controller defined in Claim 30 wherein each of the pair of compensators comprises a lead-lag compensator.

35. The controller defined in Claim 30 wherein the pair of compensators counteract a destabilizing effect of proportional gains associated with the pair of proportional controllers.

36. The controller defined in Claim 30 wherein the proportional gains reduce voltage tracking errors to a predetermined level.

37. An apparatus for supplying balanced three-phase voltages to an unbalanced three-phase load, the apparatus comprising:

an inverter coupled to the load; and

an inverter controller to control the inverter, the inverter controller comprising a synchronous frame controller in a single rotating reference frame using lead-lag compensation.

38. The apparatus defined in Claim 37 wherein the load comprises a three-wire load.

39. The apparatus defined in Claim 37 wherein the load comprises a four-wire load.

40. An apparatus for supplying balanced three-phase voltages to an unbalanced three-phase load, the apparatus comprising:

an inverter coupled to the load; and

an inverter controller to control the inverter, the inverter controller comprising a synchronous frame controller using two PI compensators in separate reference frames with opposite rotation.

41. The apparatus defined in Claim 40 wherein the load comprises a three-wire load.

42. The apparatus defined in Claim 40 wherein the load comprises a four-wire load.

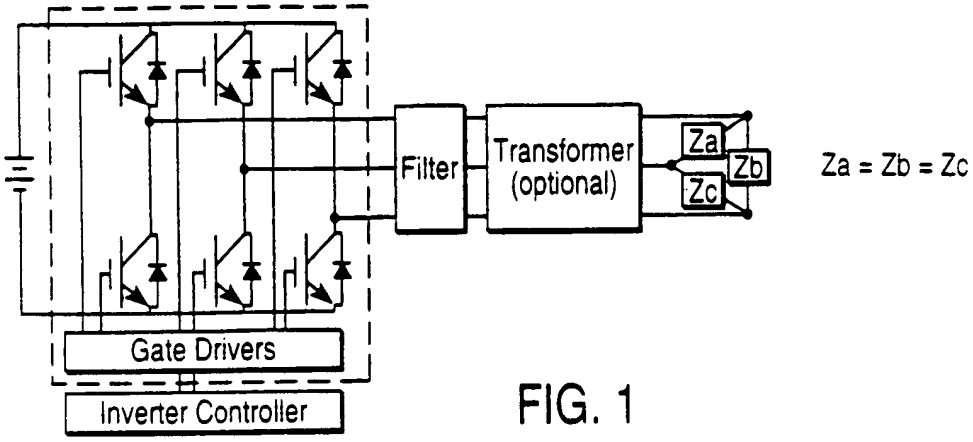

FIG. 1

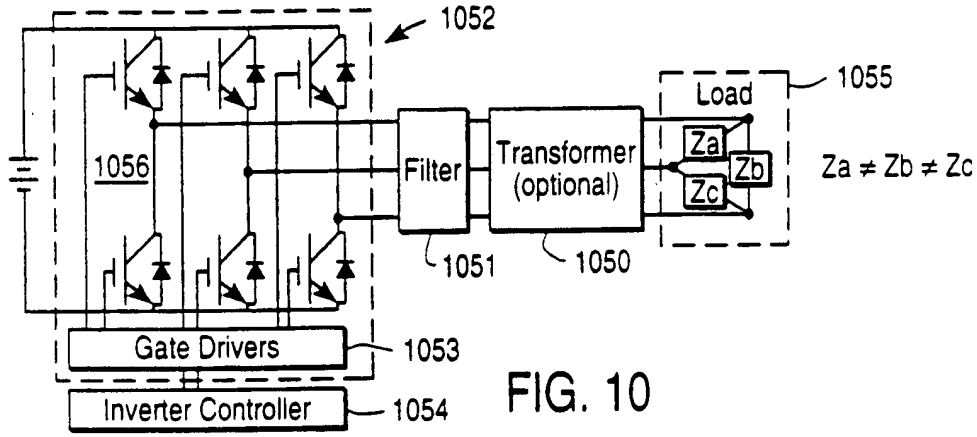

FIG. 10

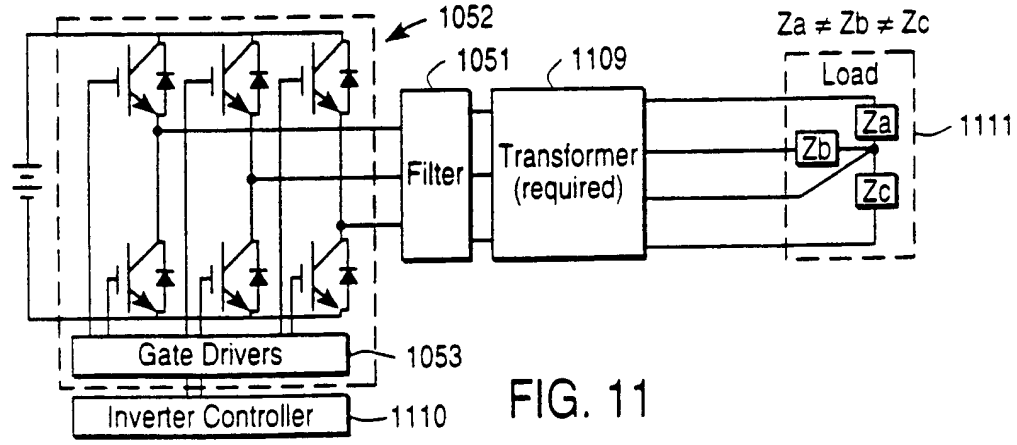

FIG. 11

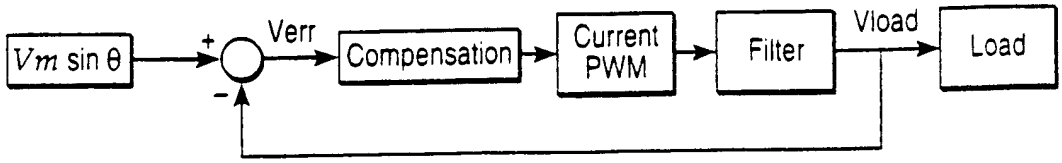

FIG. 6

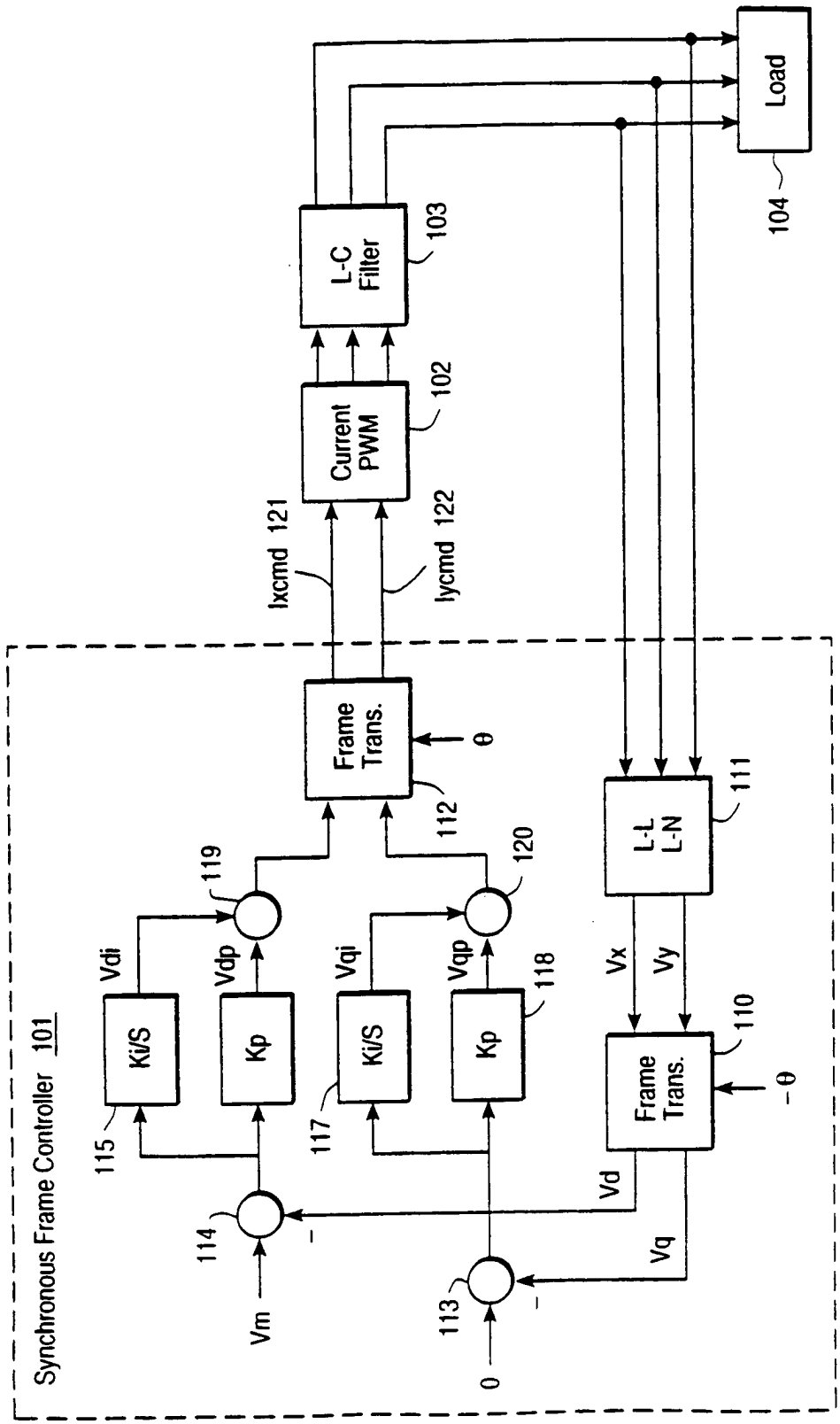

FIG. 2 Synchronous Frame PI Voltage Controller

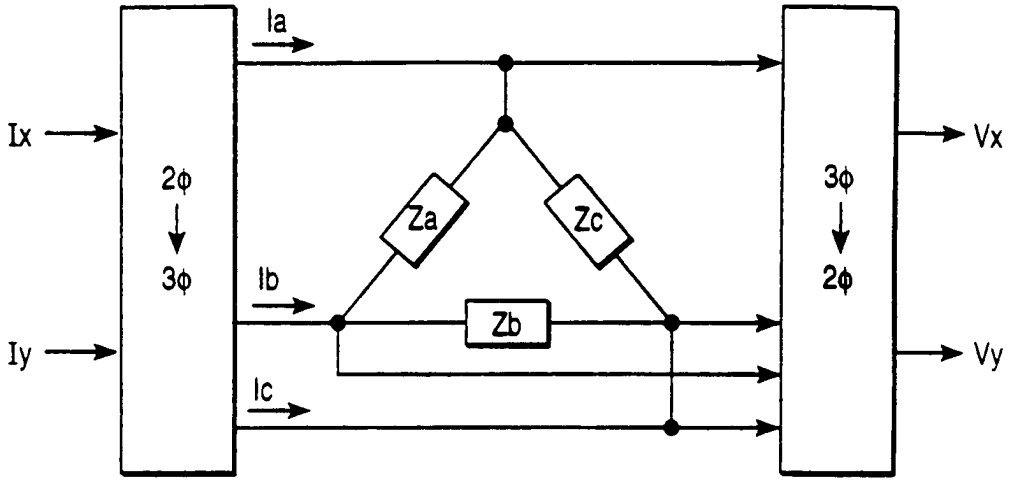
Ia
Ix
2φ
3φ
Za
Zc
Ib
Zb
Iy
Ic
3φ
2φ
Vx
Vy

FIG. 3

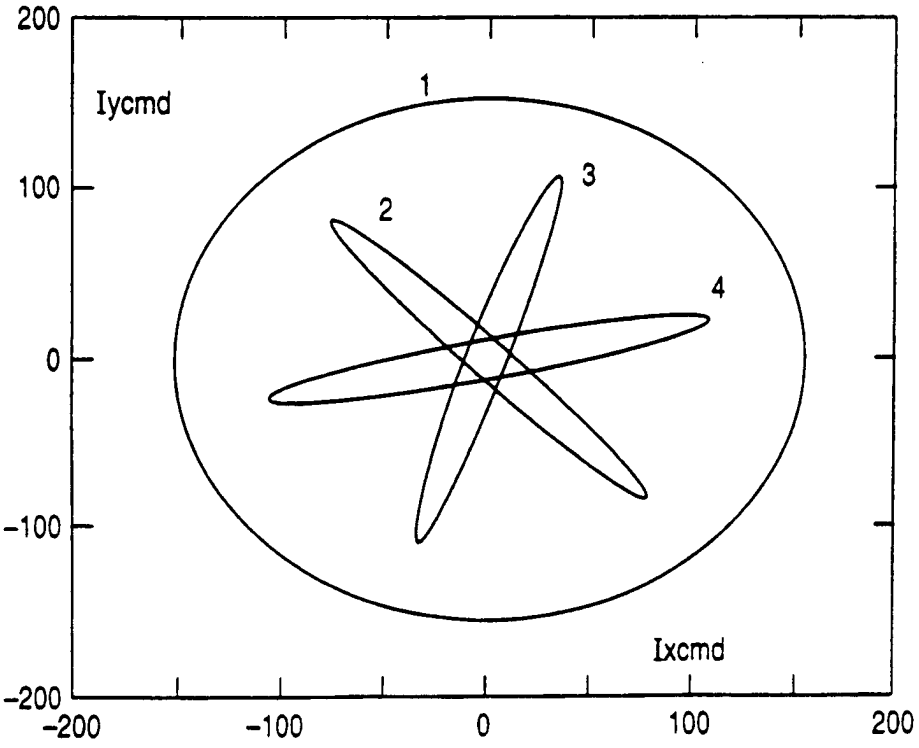
200
100
0
-100
-200
Iycmd
1
2
3
4
Ixcmd
-200
-100
0
100
200

FIG. 4

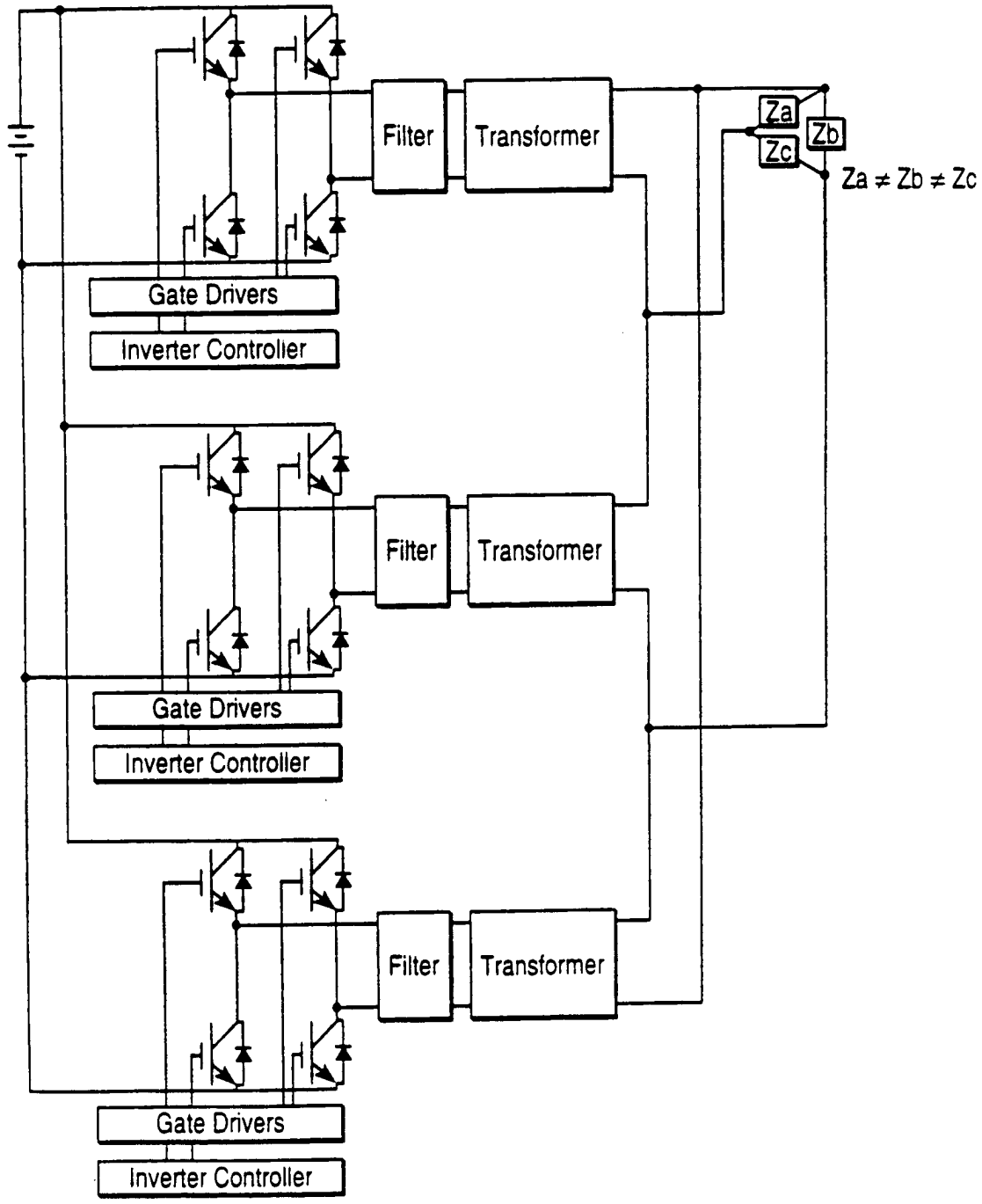
Filter
Transformer
Za
Zb
Zc
Za ≠ Zb ≠ Zc
Gate Drivers
Inverter Controller
Filter
Transformer
Gate Drivers
Inverter Controller
Filter
Transformer
Gate Drivers
Inverter Controller

FIG. 5

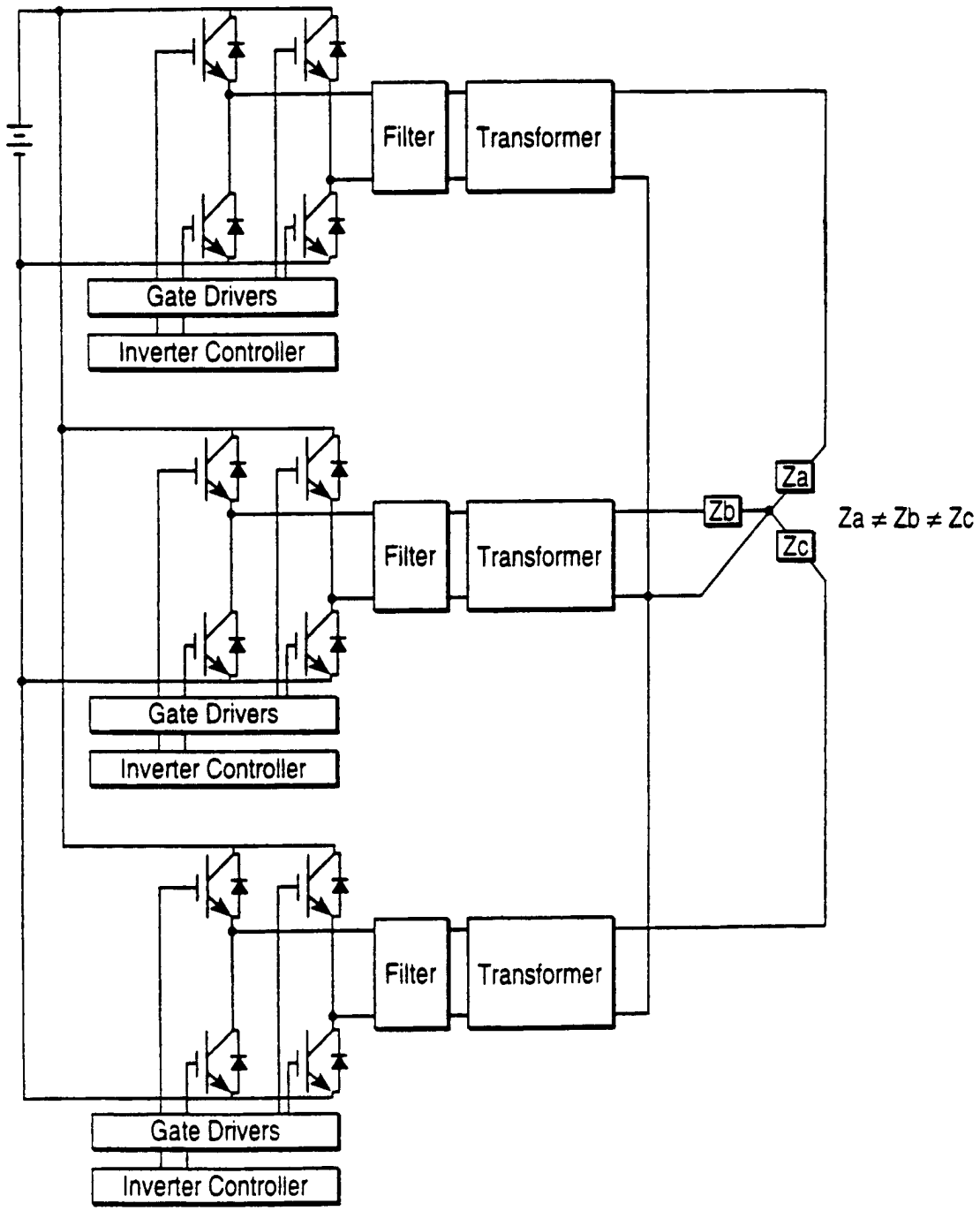
Filter
Transformer
Gate Drivers
Inverter Controller
Filter
Transformer
Gate Drivers
Inverter Controller
Filter
Transformer
Gate Drivers
Inverter Controller
Za
Zb
Zc
Za ≠ Zb ≠ Zc

FIG. 7

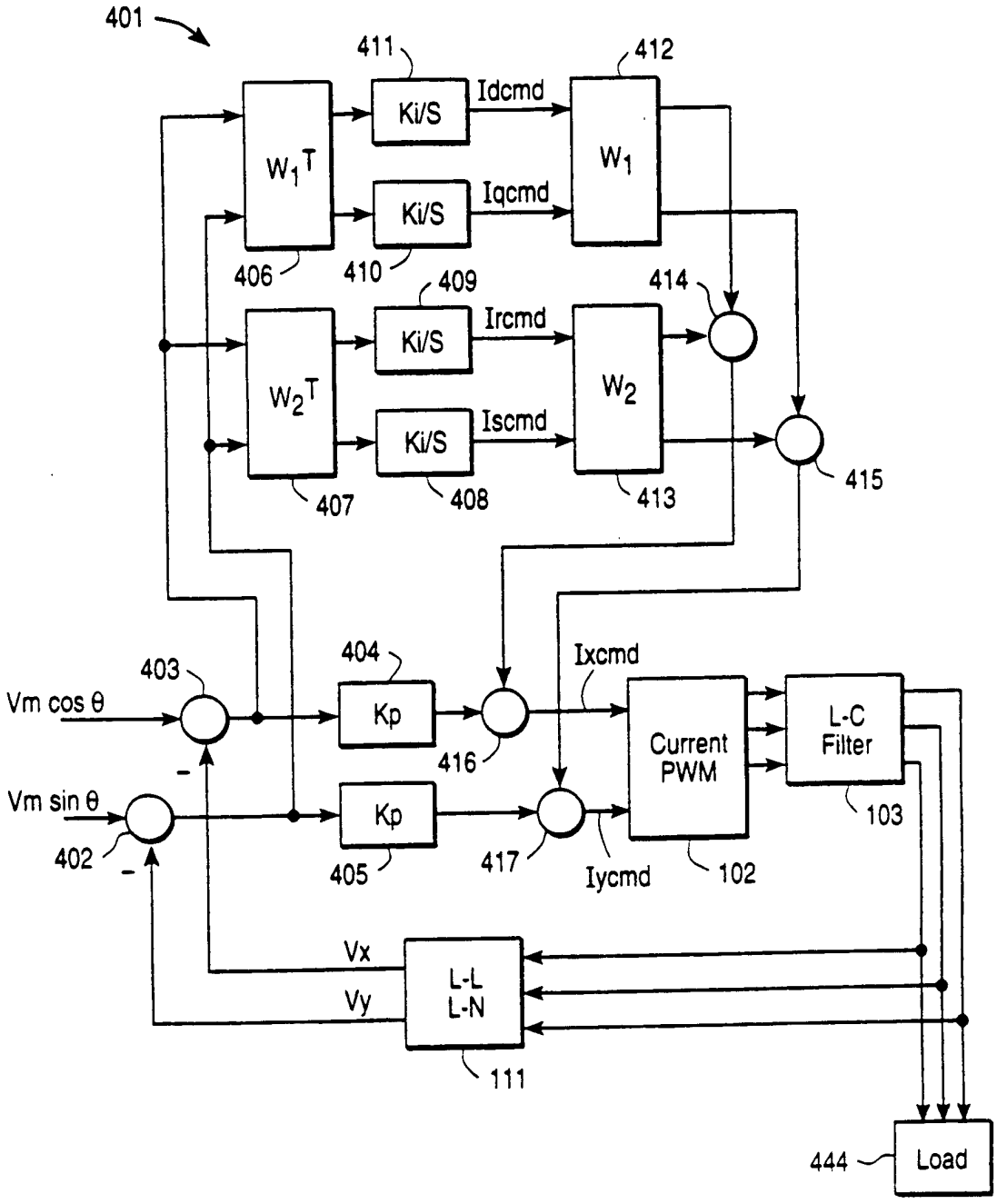
401
411
412
Ki/S
Idcmd
W_1^T
W_1
Ki/S
Iqcmd
406
410
409
414
Ki/S
Ircmd
W_2^T
W_2
Ki/S
Iscmd
415
407
408
413
403
404
Ixcmd
Vm cos θ
Kp
416
Current PWM
L-C Filter
Vm sin θ
Kp
402
405
417
Iycmd
102
103
Vx
L-L L-N
Vy
111
444
Load

FIG. 8

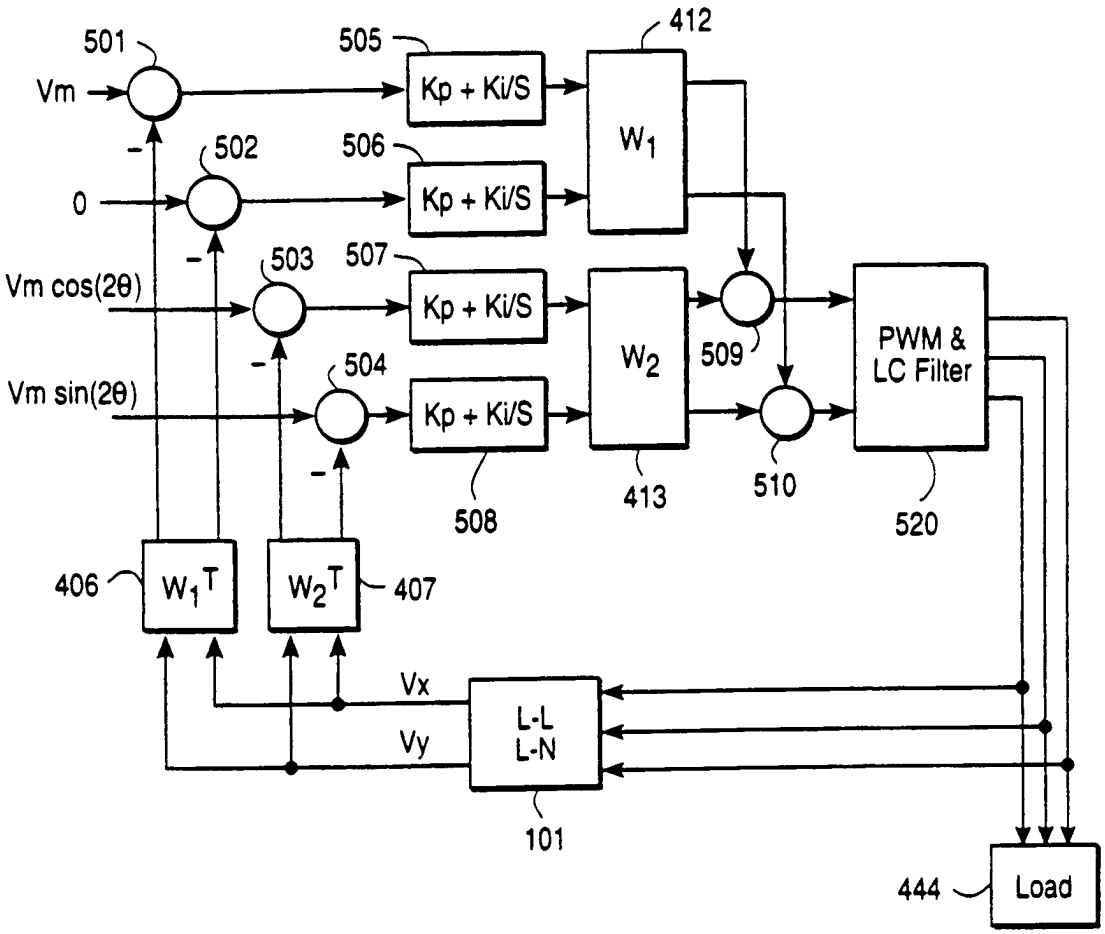
501
Vm
505
Kp + Ki/S
412
W1
502
0
506
Kp + Ki/S
503
Vm cos(2θ)
507
Kp + Ki/S
W2
509
PWM &
LC Filter
504
Vm sin(2θ)
Kp + Ki/S
508
413
510
520
406
W1T
W2T
407
Vx
Vy
L-L
L-N
101
444
Load

FIG. 9

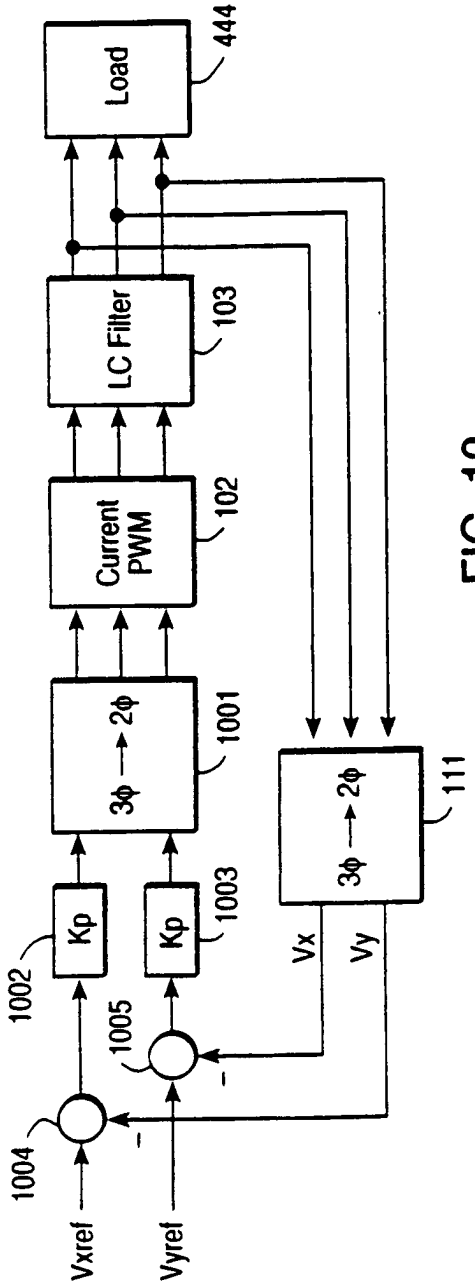
Load
444
LC Filter
103
Current PWM
102
3φ → 2φ
1001
Kp
1002
Kp
1003
3φ → 2φ
111
1004
1005
Vxref
Vyref
Vx
Vy

FIG. 12

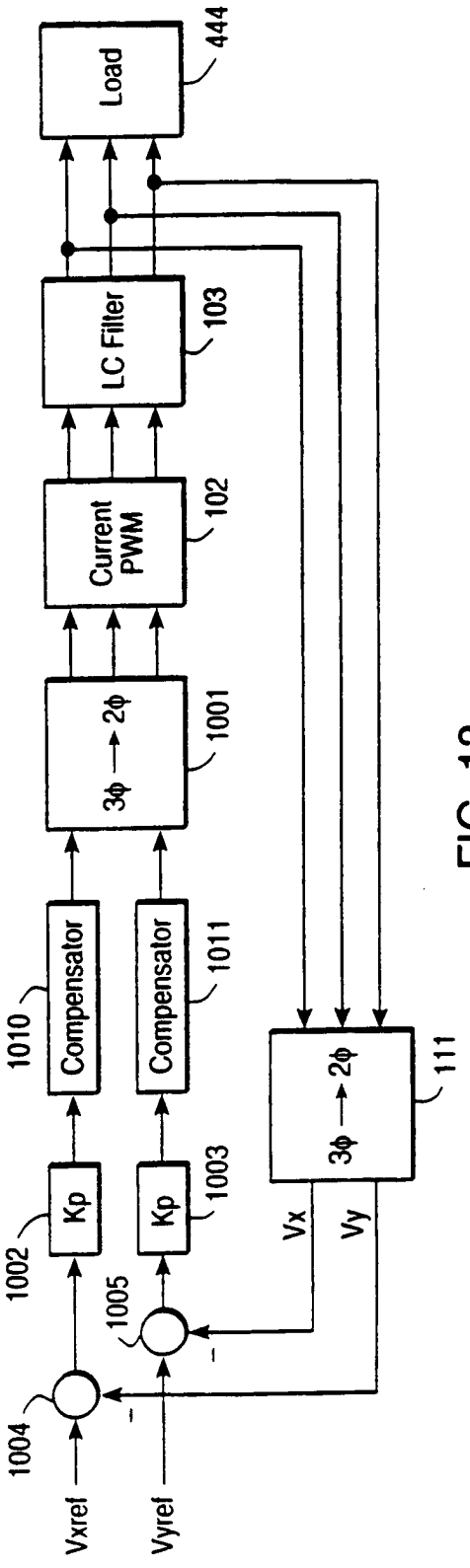
Load
444
LC Filter
103
Current PWM
102
3φ → 2φ
1001
Compensator
1010
Compensator
1011
Kp
1002
Kp
1003
3φ → 2φ
111
1004
1005
Vxref
Vyref
Vx
Vy

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/01576

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H02M 1/12
US CL :363/71,98

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 363/71,98

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
X,E	US 5,883,796 A (CHENG et al) 16 March 1999, figures 16a-c, col. 29, line 60 through col. 30, line 38.	26, 28-33, 35, 36NO
X --- Y	US 4,864,487 A (SCHNETZKA, II et al) 05 September 1989, col. 5, lines 28-47.	26-36
Y	US 5,384,696 A (MORAN et al) 24 January 1995, see entire document.	1-40
A	US 5,513,090 A (BHATTACHARYA et al) 30 April 1996.	1-42
A	US 5,648,894 A (DE DONCKER et al) 15 July 1997.	1-42

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search

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